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(54) RECEIVING/REPRODUCING DEVICE FOR DIGITAL IMAGE SIGNAL

(57)Abstract:

PURPOSE: To perform decoding adaptively while suppressing the deterioration of performance by storing coefficients to estimate true data in a data table.

CONSTITUTION: A frame disassembling circuit 13 separates reproduced data supplied from an input terminal 21 into a dynamic range DR, a minimum value MIN and quantization data DT and outputs them. Memory 22 to which the quantization data DT is supplied outputs the data of a picture element in question and that of peripheral picture elements to a class code generation circuit 23. The class code generation circuit 23 supplies a class code class representing a class

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to which the data belongs to a ROM table 24, and outputs coefficient data to estimate the true data to an estimation arithmetic circuit 25 setting the class as a readout address. The estimation arithmetic circuit 25 calculates the data near to truth of the remarked picture element by the coefficient data and the data of the remarked picture element and that of the peripheral picture elements outputted from the memory 22, and outputs it to a decoder circuit 26. The decoder circuit 26 decodes an output signal F by the dynamic range DR and the minimum value MIN.

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CLAIMS

[Claim(s)]

[Claim 1] In reception/regenerative apparatus of the digital image signal which decoded the transmission data with which each pixel was encoded with the predetermined number of bits per block A class detection means to detect the pattern which becomes settled in the coded data of the above-mentioned attention pixel, and the coded data of two or more above-mentioned pixels, to determine the class to which this pattern belongs based on this detected pattern, and to output class detection information, A means by which detection was carried out [above-mentioned] to generate the estimate of the true coded data of the above-mentioned attention pixel for every class, Reception/regenerative apparatus of the digital image signal characterized by having a data decode means to change and output the coded data of the above-mentioned attention pixel to the coded data more near true value, according to the multiplier data supplied from the above-mentioned multiplier data storage means.

[Claim 2] They are reception/regenerative apparatus of the digital image signal characterized by having the memory in which the above-mentioned estimate generating means stores multiplier data for every class in reception/regenerative apparatus of a digital image signal according to claim 1, and obtaining the above-mentioned multiplier data by study beforehand using the coded data of an attention pixel, and the coded data of two or more pixels.

[Claim 3] Reception/regenerative apparatus of the digital image signal characterized by performing processing which carries out clipping of the coded data of the circumference pixel beyond the threshold when bigger in reception/regenerative apparatus of a digital image signal according to claim 1 than a threshold with the absolute value of the differential signal of the coded data and the coded data of a circumference pixel of the above-mentioned attention pixel.

[Claim 4] In the pattern which becomes settled in reception/regenerative apparatus of a digital image signal according to claim 1 in the coded data of the

above-mentioned attention pixel, and the coded data of two or more above-mentioned pixels The class decision to which this pattern belongs with the relative relation between the coded data of an attention pixel and the coded data of a circumference pixel is made. Reception/regenerative apparatus of the digital image signal characterized by having a data decode means to perform right data decode by shifting the value of the coded data of an attention pixel, and the value of the coded data of a circumference pixel at the time of data decode.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to reception/regenerative apparatus of the digital image signal for changing into a restoration value reception/regenerative apparatus of the digital image signal applied to recording / reproducing a digital image signal with a digital video tape recorder, and the data quantized especially.

[0002]

[Description of the Prior Art] In order to attain record / reproducible transmission rate of extent since there is much the amount of information when recording a digital video signal on record media, such as a magnetic tape, usually a digital video signal is compressed by high efficiency coding. As high efficiency coding, a digital video signal is divided into much small blocks, and ADRC, DCT (Discrete Cosine Transform), etc. which process for every block are known.

[0003] ADRC is high efficiency coding which performs coding which asked for the die NAMMIKU range specified by the maximum of two or more pixels and the minimum value which are contained in a two-dimensional block which is indicated by JP,61-144989,A, and was adapted for this die NAMMIKU range.

DCT carries out cosine conversion of the pixel within a block, it re-quantizes and variable length coding of the multiplier data obtained by the conversion is carried out further. The coding approach which vector-quantizes the difference over the average value for every block and the average value of the pixel within a block here is also proposed.

[0004] Decode of the conventional ADRC is processing which changes a quantization code into the central value of the quantization code, and adds the minimum value to central value. Drawing 6 shows the situation of decode in case a quantifying bit number is 2 as an example. The quantization code of each pixel is in any of 00, 01, 10, and 11. These quantization codes are decoded in drawing 6 by the central value shown by the black dot. The minimum value MIN of that block is added to this central value. The number of bits of a quantization code is immobilization or adjustable. The error of the restoration image to a subject-copy image increases, and a restoration image deteriorates, so that this number of bits decreases.

[0005]

[Problem(s) to be Solved by the Invention] The picture signal has strong correlation locally. Even if it divides into a small field, in the method quantized with the same step size, this correlation is saved also in the encoded data. For example, as shown in drawing 7 A, when the coded data by which block coding was carried out is observed in the field of a pixel (3x3), the value of a main pixel is 2 (10 codes), and when other pixel codes are 1 (01 codes), the true value of the coded data of an attention pixel exists within the limits of (1.5-2.0) probable in many cases. As shown in drawing 7 B, the value of an attention pixel is 2, and when the value of a circumference pixel is 3, the true value of the value of the coded data of an attention pixel exists within the limits of (2.0-2.5) probable in many cases.

[0006] Like before, it was impossible except decoding to main central value only with the value of the coded data of an attention pixel. Consequently, when there were few quantization bits, there was a problem on which degradation of an

image is conspicuous. It is possible to form the decode value of finer level by using the local correlation shown in drawing 7 .

[0007] Therefore, without increasing the record number of bits, the object of this invention forms a finer suitable decode value, and is to offer reception/regenerative apparatus of the digital image signal which can reduce a quantization error by this.

[0008]

[Means for Solving the Problem] In reception/regenerative apparatus of the digital image signal with which this invention decoded the transmission data with which each pixel was encoded with the predetermined number of bits per block The class detector which detects the pattern which becomes settled in the coded data of an attention pixel, and the coded data of two or more pixels, determines the class to which this pattern belongs based on this detected pattern, and outputs class detection information, The detected circuit which generates the estimate of the true coded data of an attention pixel for every class, They are reception/regenerative apparatus of the digital image signal characterized by having the data decoder circuit which changes and outputs the coded data of an attention pixel to the coded data more near true value according to the multiplier data supplied from the multiplier data storage means.

[0009]

[Function] Reception/regenerative apparatus of the digital image signal concerning this invention detect the pattern which becomes settled in the coded data of an attention pixel, and the coded data of two or more pixels of the circumference of it, determines the class to which that pattern belongs, and outputs class detection information. The presumed-type multiplier data which is the information for computing the true coded data of an attention pixel using the coded data of an attention pixel and the coded data of two or more pixels are stored in the multiplier data storage means for every class, and this multiplier data is outputted according to the class detection information from a class detection means. Next, the restoration image whose quality improved

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conventionally is obtained by changing the coded data of an attention pixel into the coded data more near true value, and decoding using the changed coded data according to the supplied multiplier data.

[0010]

[Example] Hereafter, one example of this invention is explained. Drawing 1 shows the rough configuration of this one example, i.e., signal processing of a digital video tape recorder. A video signal is supplied from the input terminal shown by 1, and one sample is digitized by 8 bits with A/D converter 2. The output data of this A/D converter 2 are supplied to the blocking circuit 3. In this example, the service area of one frame is divided into the block of magnitude, such as a pixel (8x8), in the blocking circuit 3.

[0011] The digital video signal by which scan conversion was carried out is supplied to the shuffling circuit 4 at the sequence of the block from the blocking circuit 3. In the shuffling circuit 4, shuffling is carried out, for example per block. The output of the shuffling circuit 4 is supplied to the block coding network 5. The block coding network 5 is compressed by re-quantizing pixel data for every block. Here, the shuffling circuit 4 may be formed after the block coding network 5.

[0012] In this example, ADRC is used as block coding. Drawing 2 shows an example of a block diagram which gives detailed explanation of an ADRC coding network as a block coding network 5. In drawing 2 , the digital signal from A/D converter 2 is supplied to the input terminal shown in 21, and it is changed into the block structure by the blocking circuit 3. The maximum detector 22, the minimum value detector 23, and a delay circuit 24 are connected to the output of the blocking circuit 3, respectively.

[0013] The maximum detector 22 detects the maximum MAX of the value of pixel data for every block, and the minimum value detector 23 detects the minimum value MIN of the value of pixel data for every block. In a subtractor circuit 25, the operation of (MAX-MIN) is carried out and a die NAMMIKU range DR is detected. In a subtractor circuit 26, the minimum value MIN is subtracted from the pixel data through a delay circuit 24. The pixel data with which this minimum value

MIN was subtracted, i.e., the pixel data which it normalized, are supplied to the quantization circuit 27.

[0014] In the quantization circuit 27, the pixel data from which the minimum value MIN was removed are adapted for a die NAMMIKU range DR, and are re-quantized. When the data level of n and the pixel within a block is set to L for bit allocation, the quantization code DT is computed by the following formulas. A dynamic range DR, the minimum value MIN, and the quantization data DT are output data of the block coding network 5.

[0015] DR=MAX-MIN+1DT= [(L-MIN +0.5) -2n / DR]

However, [ ] means cut-off processing.

[0016] The output data of the block coding network 5 are supplied to the framing circuit 6. Record data are generated from the framing circuit 6 to an output terminal 28. The framing circuit 6 generates the record data of the structure where a sink block continues while generating the parity of an error correction sign. As an error correction sign, horizontal and the product code which performs error correction coding to vertical each of the matrix-like array of data are employable, for example. As for a sink block, a sink block synchronizing signal and ID signal are added to coded data and parity. The record data with which a sink block follows the channel coding network 7 from the framing circuit 6 are supplied, and processing of coding for reducing the dc component of the supplied record data is received in the channel coding network 7.

[0017] The output data of the channel coding network 7 are changed into a bit stream, rotary head H is further supplied through the record amplifier 8, and record data are recorded as a slanting truck on magnetic tape T. Usually, although two or more rotary heads are used, since it is easy, only one head is illustrated.

[0018] The playback data taken out from magnetic tape T by rotary head H are supplied to the channel decryption circuit 12 through the playback amplifier 11, and a decryption of channel coding is performed. The output data of the channel decryption circuit 12 are supplied to the frame decomposition circuit 13, and

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separation and the error correction of various kinds of data of record data are made. The error flag which shows the existence after carrying out an error correction besides playback data is contained in the output data generated from the frame decomposition circuit 13.

[0019] The output data of the frame decomposition circuit 13 are supplied to the important word correction circuit 14. The important word correction circuit 14 corrects the important word (namely, a die NAMMIKU range DR and the minimum value MIN for every block) it is indicated to be by the error flag that it is an error. Here, when an error cannot be corrected, as for the important word correction circuit 14, what has the function to presume an important word is desirable. The output data of the important word correction circuit 14 are supplied to the block decoder circuit 15. This block decoder circuit 15 performs ADRC decode using the important word in which ADRC decode was performed using the important word which is not an error, and the important word was corrected in the important word correction circuit 14 about the block of an error. The block decoder circuit 15 generates a decode value like the after-mentioned by the prediction operation using the prediction coefficient data beforehand gained and memorized by study.

[0020] The decode data of the block decoder circuit 15, i.e., each pixel and corresponding restoration data, are supplied to the DISHAFU ring circuit 16. This DISHAFU ring circuit 16 is as complementary as the shuffling circuit 4 by the side of record, and processing which returns the spatial location of a block to the original location is performed. The output data of the DISHAFU ring circuit 16 are supplied to the block decomposition circuit 17. In the block decomposition circuit 17, the sequence of data is returned to the sequence of a raster scan. The output data of this block decomposition circuit 17 are supplied to the error interpolation circuit 18. The error interpolation circuit 18 performs error detection per pixel, and interpolates the pixel data detected as an error by surrounding pixel data.

[0021] As interpolation processing, the interpolation circuit of the two-dimensional direction and the interpolation circuit of the direction of time amount can use

spatial, i.e., the thing by which sequential connection was made, for example. The output data of the error interpolation circuit 18 are supplied to D/A converter 19, and correspond to an output terminal 20 with each pixel, and the restoration data of the sequence of a raster scan are obtained.

[0022] This invention is applied to the above-mentioned block decoder circuit 15. Drawing 3 is an example of the block decoder circuit 15 by this invention. Playback data are supplied to the frame decomposition circuit 13 from the input terminal shown by 21, and it dissociates from the playback data with which a die NAMMIKU range DR, the minimum value MIN, and the quantization data DT were supplied, and is taken out and outputted in the frame decomposition circuit 13. Here, in this drawing 3 , since the important word correction circuit 14 does not have the summary and direct relation of this invention, it is omitted from this graphic display.

[0023] Memory 22 is provided with the quantization data DT. Memory 22 is coded data x1 -x9 of the pixel (3x3) centering on the attention pixel which is an object for decode as shown in drawing 5 . It outputs simultaneously. x5 of a core It is an attention pixel. The output data of memory 22 are outputted to the class code generating circuit 23.

[0024] The class code generating circuit 23 is the class code class which detects the class to which the pattern belongs and shows the class by processing a formula (1) based on the coding data pattern centering on the attention pixel supplied from memory 22. The ROM table 24 is supplied. this class code class Reading appearance is carried out when reading the multiplier data of that class mentioned later from the ROM table 24, and the address is shown.

[0025]

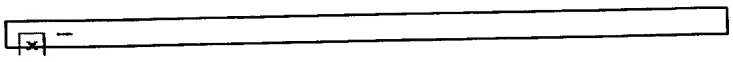
[Equation 1]

[0026] Coded data x1 -x9 integer-ized by the ROM table 24 The multiplier data for computing the coded data of the attention pixel before being integer-ized with

a pattern are memorized for every class. In addition, about the creation approach of the multiplier data memorized by the ROM table 24, it mentions later. From the ROM table 24, it is the class code class. wi which is multiplier data of the address shown to the class (class) Coding data pattern x1 -x9 inputted by being based and performing the operation shown in a formula (2) Corresponding coded data y of an attention pixel is computed. The computed data are outputted to a decoder circuit 26.

[0027]

[Equation 2]



[0028] A decoder circuit 26 is a circuit which compounds attention data. To a decoder circuit 26, a dynamic range DR and the minimum value MIN are offered from the frame decomposition circuit 13. When a decoder circuit 26 consists of a multiplication circuit and an adder circuit, and the output from the presumed arithmetic circuit 25 is set to F (above-mentioned coded data y) and it sets a quantifying bit number to n, the decode value L is shown by the degree type.

L= [(F+0.5) -DR/2n+MIN]

However, [ ] means cut-off processing. The decode value L is supplied to an output terminal 27.

[0029] Thus, an attention pixel and coded data x1 -x9 by which the circumference of it was integer-ized After asking for the multiplier data for presuming coded data y before integer-izing of a corresponding attention pixel by study beforehand for every class Coded data x1 -x9 which memorizes on the ROM table 24 and is inputted, And coded data x1 -x9 calculated and this inputted based on the multiplier data read from the ROM table 24 By forming and outputting coded data y before integer-izing of a corresponding attention pixel Coded data x5 by which the attention pixel was integer-ized Unlike the case where it only decodes, near data can be outputted with original data.

[0030] Then, the creation approach of the multiplier data stored in the ROM table

24 is explained using drawing 4 . In drawing 4 , a digital video signal is supplied to an input terminal 31, and the supplied digital video signal is supplied to the blocking circuit 32. As for the input data at this time, it is desirable that it is a standard digital video signal for training. The blocking circuit 32 carries out the same operation as the blocking circuit 3 in drawing 1 , and divides the service area of one frame into the block of the magnitude of a pixel (8x8) in this example. The ADRC circuit 33 is provided with the output signal of the blocking circuit 32.

[0031] The ADRC circuit 33 carries out the same work as the ADRC circuit 5 in drawing 1 . The output of the ADRC circuit 33 is supplied to the class code generating circuit 34 and the normal equation adder circuit 35. Among these, coded data x1 -x9 so that the field shown in the class code generating circuit 34 at drawing 5 (3x3) It is supplied and coded data y of an attention pixel is supplied to the normal-equation adder circuit 35. Coded data x1 -x9 supplied to the class code generating circuit 34 here It is the integer-ized value and coded data y supplied to the normal-equation adder circuit 35 is a value containing below decimal point before being integer-ized.

[0032] The class code generating circuit 34 is the same as the class code generating circuit 23 explained previously, by performing the operation shown in a formula (1) based on the coding data pattern supplied from the ADRC circuit 33, detects the class to which the pattern belongs, and outputs the class code which shows the class. The class code generating circuit 34 outputs a class code to the normal equation adder circuit 35.

[0033] Here, study of the transformation from two or more coded data to the coded data of an attention pixel and the signal transformation which used the prediction equation are described for explanation of the normal-equation adder circuit 35. Below, a pixel is generalized more for explanation and the case where prediction by n pixels is performed is explained. About quantization data, they are x1, ..., xn. It carries out and is the class class of this field. It defines by the formula (1).

[0034] When the quantization data level of the attention pixel which should be

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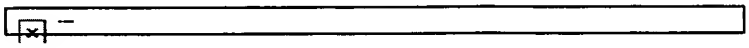
presumed is set to y, they are a multiplier, w1, ..., wn for every class. The linearity presumption type of n tap to depend is set up. This is shown in a formula (3). Before study, it is wi. It is an undetermined coefficient.

[0035]

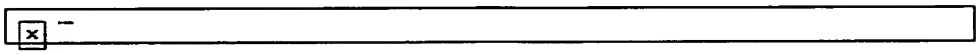
[Equation 3]



[0036] Study is performed to two or more signal data for every class. When the number of data is m, a formula (4) is set up according to a formula (3).

[0037]

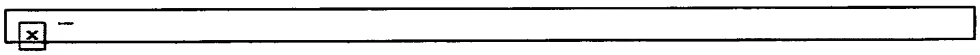
[Equation 4]



[0038] In m>n, they are w1, ..., wn. Since it is not decided that it will be a meaning, a formula (5) defines the element of the error vector e, and it asks for the multiplier which makes a formula (6) min. This is a solution method by the general least square method.

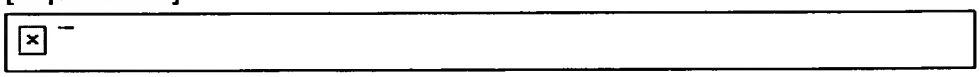
[0039]

[Equation 5]



[0040]

[Equation 6]



[0041] Here, it is wi of a formula (6). It asks for the partial differential coefficient to depend. It is each wi so that a formula (7) may be set to 0. What is necessary is just to ask.

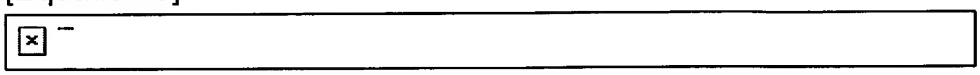
[0042]

[Equation 7]

[0043] Hereafter, it is XjiYi like a formula (8) and a formula (9). If a definition is given, a formula (7) will be rewritten by the formula (10) using a matrix.

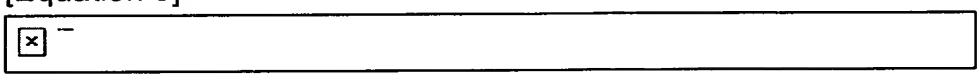
[0044]

[Equation 8]



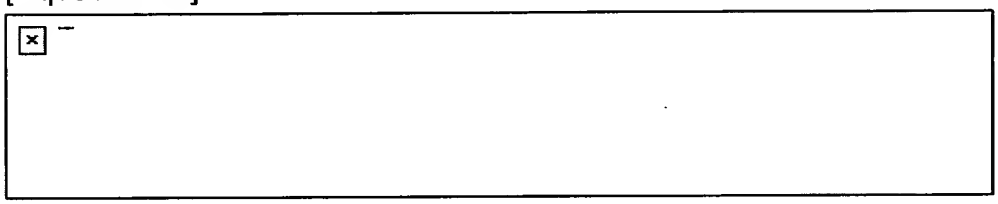
[0045]

[Equation 9]



[0046]

[Equation 10]



[0047] Generally this equation is called the normal equation. The normal equation adder circuit 35 adds this normal equation using the class code supplied from the class code generating circuit 34, the coded data x1 supplied from the ADRC circuit 33, ..., xn, and coded data y similarly supplied from the ADRC circuit before being integer-ized.

[0048] After all trainee NINGU entries of data are completed, the normal-equation adder circuit 35 outputs normal-equation data to the prediction coefficient decision circuit 36. the prediction coefficient decision circuit 36 -- a normal equation -- sweeping out -- general matrix solution methods, such as law, -- using -- wi ******** -- it solves and a prediction coefficient is computed. The prediction coefficient decision circuit 36 writes the computed prediction coefficient

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in memory 37.

[0049] As a result of training as mentioned above, in memory 37, they are the quantization data x1-x9. The prediction coefficient which can perform presumption statistical nearest to a true value for presuming attention coded data y is stored for every pattern specified. The table stored in this memory 37 is the ROM table 24 used in the picture signal regenerative apparatus of this invention as mentioned above. the above processing -- a linearity presumption type -- quantization data x1 -x9 from -- study of the multiplier data for creating attention coded data y is completed.

[0050] In addition, although the above-mentioned example was an example which carried out this invention in ADRC of a two-dimensional block, this invention is applicable also about ADRC of a three-dimension block.

[0051] In addition, although an above-mentioned example is satisfactory at the time of ADRC (about 1-2 bits) of a low bit, if it is going to apply as it is in bit allocation, the thing beyond it which the magnitude of a ROM table will become huge and feasibility becomes low will also be considered. In this case, the technique of performing a class classification may be used by using 2 bits of high orders of a quantization code, for example. The number of classes may be reduced by performing ADRC processing for **** and a quantization code further.

[0052] Moreover, as the writer proposed in the invention report 93033124, when a threshold with the absolute value of the difference is exceeded using difference with the coded data of an attention pixel, the number of classes may be reduced by performing processing which carries out clipping of the value.

[0053] Here, the explanation about clipping processing is described. First, the data-conversion circuit T which performs clipping processing is set up. In this data-conversion circuit T, the coded data of an attention pixel is first subtracted from the coded data of the circumference pixel of an attention pixel. That is, in this data-conversion circuit T, as shown in drawing 8 A, the coded data of a circumference pixel (C1, C2, C3, C4, C6, C7, C8, C9) is changed into the differential signal of the coded data of an attention pixel (C5), and the coded data

of a circumference pixel, and as shown in drawing 8 B, the coded data of a circumference pixel is changed. In addition, the signal (D1, D2, D3, D4, D6, D7, D8, D9) acquired by this conversion is henceforth called a differential signal (1-4, 6-9) D. For example, in the coded data shown in drawing 9 A, the coded data of an attention pixel, '5', is subtracted from the coded data of each circumference pixel, and it is changed into the differential signal. [i.e.,] That is, it is changed into the coded data shown in drawing 9 B. Moreover, the coded data shown in drawing 10 A is changed into the coded data shown in drawing 10 B.

[0054] In a place, coded data is restricted to the value of (0-15) in for example, the 4-bit fixed length's ADRC example. Therefore, a differential signal (1-4, 6-9) D can take a value [respectively / (-15-+15)]. However, when the class code corresponding to all these differential signals is supplied to the ROM table 24, the magnitude of the ROM table 24 will become huge. Moreover, since correlation of a pixel is a part with the part weak from the first with the big differential signal of the coded data of an attention pixel, and the coded data of a circumference pixel, to such a pattern, the effectiveness of quantization error relief is low.

[0055] So, in the data-conversion circuit T, when the absolute value of a differential signal (1-4, 6-9) D exceeds a certain threshold Th, processing which carries out clipping of the value is performed. For example, the value is changed into '5' when threshold Th is '5', and a differential signal is larger than '5'. Moreover, the value is changed into '-5' when a differential signal is smaller than '-5'. For example, when the small coded data of a differential signal as shown in drawing 9 B, i.e., the coded data considered that correlation of an image is strong, is contained in a block, conversion of a differential signal is not performed in the data-conversion circuit T. On the other hand, when the large coded data of a differential signal as shown in drawing 10 B, i.e., the coded data considered that correlation of an image is weak, is contained in a block, in the data-conversion circuit T, clipping processing is performed only to the large part of a differential signal. That is, the coded data of drawing 10 B is changed into the coded data of drawing 10 C.

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[0056] This clipping processing is performed, for example between the ADRC circuit 33 of drawing 4 , and the class code generating circuit 34 at the time of the multiplier data origination stored in the ROM table 24, for example between the memory 22 of drawing 3 , and the class code generating circuit 23 at the time of the usual signal processing.

[0057] The level difference of data is an intense part and the pattern which clipping was carried out and disappeared on the other hand is a pattern with the thin relief effectiveness of a quantization error from the first. Therefore, even if it decreases the number of patterns substantially, the performance degradation of a quantization error is slight and ends.

[0058] Next, the shift of coded data at the time of data decode is explained. Although [the quantization data C5 of the above-mentioned attention pixel] it has the value to (0-15) as it is, the quantization data C5 of an attention pixel prepare only the multiplier data in '0' in the ROM table 24. When the quantization data C5 of an attention pixel are '2', the quantization data which are an attention pixel are shifted to '0' from '2'. The quantization data of the circumference pixel within the same block also shift only the same shift amount. Based on the class of the shifted pattern, multiplier data are read from the ROM table 24. Coded data y before integer[to which the attention pixel was shifted]-izing corresponding to the data which performed the operation shown in a formula (2) and shifted the inputted data to C1-C9 is formed and outputted, and the reverse shift of each data is carried out at the time of data decode.

[0059] Shift processing of this coded data is performed between the memory 22 of drawing 3 , and the class code generating circuit 23.

[0060]

[Effect of the Invention] In this invention, since the number of bits transmitted can have a step with fine decode level at least, a quantization error and block distortion can be decreased and a restoration image can be made good. Moreover, since this invention performs adaptation compound based on local correlation of an image, S/N is improvable, holding space resolution. Furthermore,

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this invention does not need to transmit a special code and has an efficient advantage.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram of record/regenerative circuit of the digital video tape recorder which can apply this invention.

[Drawing 2] It is the block diagram showing an example of the configuration of the ADRC coding network which can apply this invention.

[Drawing 3] It is the block diagram showing an example of the configuration of the block decoder circuit to which this invention was applied.

[Drawing 4] It is the block diagram showing the configuration at the time of training for creating the ROM table in one example of this invention.

[Drawing 5] It is approximate line drawing for explanation of actuation of this invention.

[Drawing 6] It is drawing for explaining an example of quantization of ADRC.

[Drawing 7] It is drawing for explaining the principle of this invention.

[Drawing 8] It is approximate line drawing for explaining the pattern data deformation method of this invention.

[Drawing 9] It is approximate line drawing for explaining the pattern data deformation method of this invention.

[Drawing 10] It is approximate line drawing for explaining the pattern data deformation method of this invention.

[Description of Notations]

15 Block Decoder Circuit

24 ROM Table